Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A deep trench capacitor memory cell, comprising:

a first conductivity type semiconductor substrate with a main surface;

a second conductivity type ion implantation well with a well junction depth located on said main surface;

a gate dielectric layer located on said ion implantation well;

a gate located on said gate dielectric layer;

a heavily doped S/D region of said first conductivity type disposed at one side of said gate in said ion implantation well;

a lightly doped drain (LDD) region of said first conductivity type disposed at the other side of said gate in said ion implantation well; and

a deep trench capacitor vertically extending into said main surface through said well junction depth of said ion implantation well to a pre-selected depth, wherein said deep trench capacitor, which is fabricated adjacent to said LDD region, comprises an ion out diffusion well of said second conductivity type that is formed at a lower portion of said deep trench capacitor and is merged with

said ion implantation well, and a conductive electrode pillar electrically isolated from said LDD region, said ion implantation well, and said ion out diffusion well by a capacitor dielectric layer and a trench top insulation layer.

[c2] 2.The deep trench capacitor memory cell according to claim 1 wherein said first conductivity type is P type, and said second conductivity type is N type.

[c3] 3.The deep trench capacitor memory cell according to claim 1 wherein said ion out diffusion well has a top end located a depth of about 4000~6000 angstroms below said main surface of said substrate.

[c4] 4.The deep trench capacitor memory cell according to claim 1 wherein said deep trench capacitor vertically extends into said main surface through said well junction depth of said ion implantation well to a depth that is deeper than 3 micrometers.

[c5] 5.The deep trench capacitor memory cell according to claim 1 wherein said capacitor dielectric layer is an oxide-nitride-oxide (ONO) dielectric layer.

[c6] 6.The deep trench capacitor memory cell according to claim 1 wherein said trench top insulation layer is made of silicon oxide.

[c7] 7.The deep trench capacitor memory cell according to claim 6 wherein said trench top insulation layer is disposed atop said conductive electrode pillar and has thickness of about 100~400 angstroms.

[c8] 8.A deep-trench 1T-SRAM device, comprising:
a PMOS transistor formed on an N-type ion implantation well, wherein said N-type ion implantation well is formed on a surface of a P-type semiconductor substrate, wherein said PMOS transistor comprises a gate located on said N-type ion implantation well, a gate dielectric layer interposed between said gate and said N-type ion implantation well, a P^+ source/drain region disposed at one side of said gate in said N-type ion implantation well, and a P-type lightly doped region (LDD) region disposed in said N-type ion implantation well at the other side of said gate that is opposite to said P^+ source/drain region; and
a deep trench capacitor vertically extending into said surface of said semiconductor substrate and penetrating through said well junction depth of said ion implantation well to a pre-selected depth, wherein said deep trench capacitor, which is fabricated adjacent to said P-type LDD region, comprises an N^+ ion out diffusion well that is formed at a lower portion of said deep trench capacitor and is merged with said N-type ion implantation well,

and a conductive electrode pillar electrically isolated from said P-type LDD region, said N-type ion implantation well, and said N^+ ion out diffusion well.

[c9] 9.The deep-trench 1T-SRAM device according to claim 8 wherein a trench top insulation layer is disposed atop said conductive electrode pillar.

[c10] 10.The deep-trench 1T-SRAM device according to claim 9 wherein a share contact plug penetrates through said trench top insulation layer and is electrically connected to said conductive electrode pillar.

[c11] 11.The deep-trench 1T-SRAM device according to claim 9 wherein said trench top insulation layer is made of silicon oxide.

[c12] 12.The deep-trench 1T-SRAM device according to claim 11 wherein said trench top insulation layer has a thickness of about 100~400 angstroms.

[c13] 13.The deep-trench 1T-SRAM device according to claim 8 wherein said capacitor dielectric layer is an oxide-nitride-oxide (ONO) dielectric layer.

[c14] 14.The deep-trench 1T-SRAM device according to claim 8 wherein said deep trench capacitor vertically extends into said surface through said well junction depth of said

ion implantation well to a depth that is deeper than 3 micrometers.